(6)

Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN

[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]

Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 50017

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2025

Fifth Semester

Computer Science and Engineering

U23CS514 – MICROPROCESSOR AND MICROCONTROLLER

(Common to IT)

(Regulation 2023)

Time: Three Hours   Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Define Minimum Mode and Maximum Mode of the 8086 and state two differences between them.	2	K2	CO1
2.	Differentiate Immediate addressing and Based Indexed addressing in 8086; give one short example assembly syntax for each.	2	K2	CO1
3.	State the purpose of the 8255A control word and enumerate two typical control-word configurations.	2	K2	CO2
4.	Identify the function of ICW1–ICW4 in 8259A initialization and state the significance of the cascade lines.	2	K2	CO2
5.	List the contents of the 8051 Program Status Word (PSW) and identify two flag bits with their use.	2	K1	CO3
6.	Sketch the 8051 opcode fetch cycle signals (ALE, PSEN, RD, WR) and state the role of ALE briefly.	2	K2	CO3
7.	Compute the TH1 reload value required for serial transmission at 9600 baud using Timer 1 in Mode 2 for a 11.0592 MHz crystal.	2	K2	CO4
8.	State two differences between Timer Mode and Counter Mode in the 8051 timers.	2	K2	CO4
9.	Enumerate the signal lines and their functions required to interface an external ROM to the 8051.	2	K1	CO5

			Marks	KL	CO
10.		List two advantages and two limitations of using an 8279 for keyboard/display interfacing with a microcontroller.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Illustrate the Intel 8086 architecture with a labeled block diagram. Critically analyze how the Bus Interface Unit (BIU) and Execution Unit (EU) cooperate to improve instruction throughput.	13	K1	CO1
		(OR)			
	b)	Design an 8086-assembly routine that reverses a block of bytes of length N in-place (DS:SI points to block, N in CX). Present the algorithm, assembly code with concise comments and analyze its time complexity	13	K3	CO1
12.	a)	Develop the initialization sequence and control-word scheme to configure 8255A for the following: Port A input, Port B output, Port C upper nibble output, Port C lower nibble input. Provide the control word, explain the rationale and give one application where this configuration is useful.	13	K2	CO2
		(OR)			
	b)	Construct an interfacing and priority-plan for connecting two external devices (Device A — vectored, Device B — non-vectored) to an 8086-system using 8259A. Include initialization bytes and justify the priority arrangement.	13	K2	CO2
13.	a)	Analyze the 8051-memory organization and register-bank mechanism. Propose a register-bank usage strategy for an interrupt-heavy application and justify your proposal.	13	K3	CO3
		(OR)			
	b)	Formulate an 8051-assembly subroutine that implements a signed 16-bit addition (operands in R0–R1 and R2–R3, result in R4–R5). Provide the code, indicate addressing modes used and validate correctness with one example.	13	K3	CO3
14.	a)	Design an 8051-based firmware approach to generate a variable-frequency PWM output on P1.0 controlled via serial commands. Provide block-level flow, timer configuration, and an outline of the command parsing routine.	13	K3	CO4
		(OR)			
	b)	Develop an interrupt-driven serial transmit/receive scheme for 8051 to implement full-duplex ASCII communication. Provide the initialization steps, ISR behavior (concise), and evaluate advantages over polling-based method.	13	K3	CO4

Q.No.		Questions	Marks	KL	CO
15.	a)	Design the hardware and software interface for connecting an 8-bit ADC (e.g., ADC0808/0809) to 8051 for periodic sensor sampling. Provide the signal timing sequence, pseudo-assembly routine for conversion and data retrieval, and analyze how sampling rate is determined.	13	K3	CO5
		(OR)			
	b)	Construct an address decoding circuit (logic equations and sketch) to map a 16K × 8 external ROM at 0x8000–0xBFFF with the 8051. Explain required control signals and assess the effect if ALE timing is not handled correctly.	13	K3	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	A development team must build a prototype access-control keypad with display and logging using an 8051 microcontroller. The system requirements: scan a 4×4 matrix keypad, display prompts on a 16×2 LCD, log each successful access with a timestamp into external ROM (readable later), and communicate events to a PC over RS-232. Propose a complete system solution covering hardware block diagram (key components and interconnections), address map for external memory, keypad scanning algorithm (no detailed code but clear pseudo-steps), LCD control sequence, serial configuration, and power/interrupt considerations. Evaluate potential bottlenecks and propose mitigation strategies.	15	K3	CO4
		(OR)			
	b)	Given an 8086-based legacy controller that must now interface to a modern peripheral that uses serial communication and DMA-like bulk transfer, propose an upgraded interface scheme using 8251A (serial), 8255A and 8253 where appropriate. Provide the system block diagram, explain data flow for a bulk transfer from peripheral to memory, describe necessary 8259A changes for interrupt handling, and assess timing/throughput constraints that may affect real-time performance.	15	K2	CO2